

A Squarer Circuit's Topological Innovations for Signal Processing Transcendence

Ahmed Hassan Mohammed, Department of Electrical Engineering, Shirqat Engineering College, Tikrit University, Iraq

Abstract: In this study, we embark on an exploration of the versatile applications of a CMOS squaring circuit, unveiling its potential as an invaluable asset in the realm of analog signal processing. The reconfigurable nature of this circuit bestows upon it a remarkable malleability, rendering it a fundamental analog cell, a veritable canvas upon which a myriad of building blocks can be meticulously crafted. These building blocks encompass a diverse array of functionalities, including multipliers, logarithmic modules, dividers, and exponential function generators, each a vital component in the symphony of analog signal manipulation. Moreover, this innovative circuit presents an ingenious solution for the implementation of analog logarithmic and exponential functions, characteristics that have long eluded seamless integration into CMOS technology. In pursuit of a comprehensive understanding of this circuit's performance, we delve into the intricate effects of channel-length modulation and the inherent mismatch in threshold voltages, meticulously dissecting these phenomena to unravel their impact on the circuit's behavior. The proposed circuits have been meticulously designed and simulated using the industry-standard HSPICE simulator, leveraging the level 49 parameters (BSIM3v3) tailored for 0.35 μm standard CMOS technology. Furthermore, the simulation results have been validated through rigorous analysis and cross-referencing with MATLAB-derived data, ensuring the utmost accuracy and reliability of our findings.

Keywords: Squarer, Analog modulation, MOS, Signal processing, Mathematical function.

Introduction

In the contemporary landscape of analog signal processing, computational circuits have emerged as indispensable workhorses, their versatility enabling the realization of a myriad of mathematical functions that undergird numerous applications [1]-[7]. The exponential function, a paragon of utility, finds its calling in the realms of telecommunications, medical equipment, disk drives, and hearing devices, its influence permeating a diverse array of domains [1]-[3]. Concurrently, the squaring and multiplication stand as fundamental blocks, their presence woven into the very fabric of applications in signal processing such as modulator, frequency doubling, phase locked loop, as well as the intricate architectures of fuzzy controllers [4], [5]. In addition, systems predicated upon the principles of neural network demand the integration of division functionality within their output stage, a critical component aptly termed the defuzzification block [6]. Simultaneously, in the realm of analog signal processors (ASPs), the logarithmic function assumes a pivotal role, its implementation enabling the realization of logarithmic amplifiers [7]. Concomitantly, an overarching aspiration within the domain of integrated analog designs is the pursuit of modularity, wherein a single cell can be harnessed for multiple applications. This paradigm of reusability holds the promise of significantly reducing the design costs associated with each implemented function, a tantalizing prospect

that has catalyzed the exploration of novel architectures. In this vein, the squaring circuit emerges as a preeminent candidate for the role of a "basic cell," its versatility and utility rendering it a valuable asset. This circuit has been realized through a panoply of approaches. The first draws upon the characteristics of square-law inherent to MOS operating within the region of saturation [9], [10]. The other method harnesses the capabilities of multipliers to derive desired squarer, albeit at the cost of an increased transistor count. An alternative methodology employs a judicious combination of voltage shift system. Also, the method of low voltage imposes constraints on the achievable operating frequency in certain transistors [11]. Additionally, novel circuits have been proposed, wherein voltage signals are accepted as inputs, and current signals are produced as outputs [8]. These circuits exhibit a commendable simplicity of structure, requiring fewer transistors, yet necessitating the integration of threshold voltage generator circuits. The circuit presented in [4] leverages the trans linear loop principle, thereby attaining a desirable combination of wide bandwidth and high dynamic range. However, this architecture necessitates the inclusion of auxiliary circuits to generate the requisite input signals, a consequence of which is an increased power dissipation profile. Within the pages of this scholarly endeavor, we embark on an exploration of the multifaceted applications of a current-mode squaring circuit, unveiling its prowess as an invaluable asset in the realm of analog signal processing. This pioneering circuit architecture finds its foundation in the intricate interplay of dual trans linear loops, harnessing their synergy as a "basic cell" from which a myriad of computational circuits can be realized. Design experiences garnered over years of dedicated inquiry have illuminated the significant advantages that circuits predicated upon "dual trans linear loops" – an architectural paradigm that harmoniously weaves together N-channel and P-channel transistors – can present when compared to their conventional counterparts. These latter structures, constrained by the utilization of either NMOS or PMOS transistors alone, often exhibit limitations of speed as well as dynamic range [13]-[16]. In contrast, the "dual trans linear loop" approach transcends these boundaries, ushering in a new era of enhanced performance. This cell is meticulously design to realize a diverse array of blocks that form the bedrock of analog signal processors. These include multipliers, dividers, logarithmic modules, and exponential function generators, each a vital component in the intricate symphony of analog signal manipulation. By harnessing the power of this reconfigurable cell, these elusive functions can now be seamlessly woven into the fabric of a unified, configurable architecture. The current-mode implementation of these circuits offers a path of elegant simplicity, yielding configurations that are both intuitive and straightforward, thereby facilitating their practical realization and integration into larger systems. The performance of these circuits has been meticulously characterized using the industry-standard simulators, operating in 3.3V and leveraging the TSMC level 49 (BSIM3v3) parameters tailored for the 0.35 μ m CMOS technology node. This comprehensive characterization ensures a thorough understanding of the circuits' behavior, paving the way for their seamless integration into practical applications.

Explanation of Main Cell

Figure 1 demonstrates the circuit of squarer which is used in the main cell and contain a loop of transistor M1 to M4 [14]. When operating within saturation region, and by judiciously discounting the secondary effects of modulation and mobility, the drain current of a PMOS transistor can be analytically expressed as:

$$I_{SD} = K_p (V_{SG} - |V_{tp}|)^2 \quad (1)$$

$$V_{SG} = |V_{tp}| + \sqrt{\frac{I_{SD}}{K_p}} \quad (2)$$

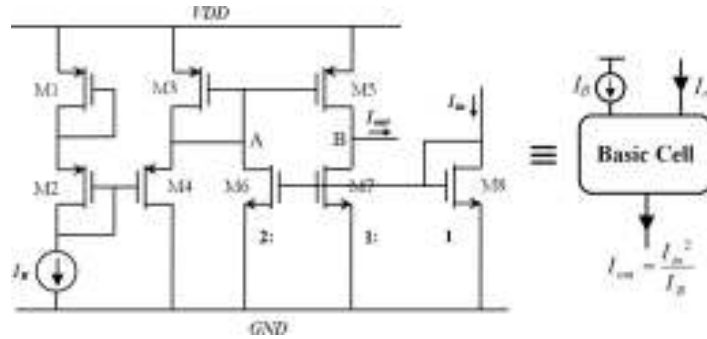


Fig. 1. The circuit of squarer which used as the main circuit [15].

This elegant formulation encapsulates the fundamental relationship that underpins the cell's operation, providing a theoretical framework upon which the architectural intricacies are meticulously constructed. However, it is prudent to note that in practical realizations, the influence of these secondary effects cannot be entirely neglected, necessitating a nuanced consideration of their impact on the circuit's performance characteristics. With this theoretical bedrock firmly established, we turn our focus to the exquisite choreography that unfolds within the dual translinear loop, where currents and voltages engage in a delicate equilibrium, orchestrating the realization of the squaring function with remarkable precision.

Let us consider the exquisite equilibrium that unfolds within the loop comprising M1 transistor through M4. We arrive at the following elegant relationship:

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \quad (3)$$

M1 through M4 shows a loop of translinear, each operate within the saturation regime. Invoking the foundational principles elucidated in (1) and (2), and acknowledging the condition $I_{SD1} = I_{SD2} = I_B$, we can derive:

$$\sqrt{I_{SD1}} + \sqrt{I_{SD2}} = \sqrt{I_{SD3}} + \sqrt{I_{SD4}} \quad (4)$$

This analytical expression encapsulates the delicate balance that must be maintained within the dual translinear loop, a harmony that underpins the circuit's operation.

To witness the resonance of precision that this architectural paragon achieves, let us turn our attention to the simulation results depicted in Fig. 2. Here, we observe the signal in the input which its frequency is 1MHz, its corresponding signal at the output, and the meticulous quantity of error – a testament to the circuit's unyielding pursuit of accuracy.

$$\sqrt{I_{SD1}} + \sqrt{I_{SD2}} = \sqrt{I_{SD3}} + \sqrt{I_{SD4}} \quad (5)$$

$$I_{SD} = K_p (V_{SG} - |V_{tp}|)^2 \quad (6)$$

Then we have these expressions as the follow:

$$16I_B^2 - 16I_B I_{out} + 4I_{out}^2 = 4I_{out}^2 - 4I_{in}^2 \quad (7)$$

The output current of the circuit can thus be elegantly expressed as:

$$I_{out} = \frac{I_{in}^2}{4I_B} + I_B \quad (8)$$

This iconic relationship, encapsulated in (8), represents the squarer of current which we expected this result. It is noteworthy that the output current will be harnessed in the form of I_{in}^2/I_B , facilitated by the judicious integration of circuit of current copier, meticulously dimensioned to achieve the desired outcome.

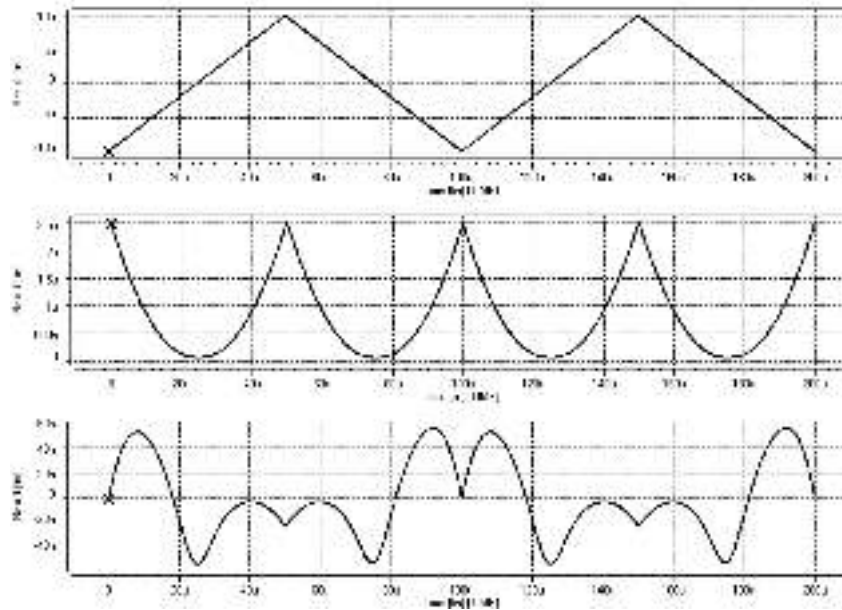


Fig. 2. The results of the proposed circuit: a) input, b) output and c) error

Applications in Processing of Signal in Analog Mode

With the circuit of figure 1 as our architectural cornerstone, and the judicious integration of additional current mirrors whenever necessary, we can orchestrate a symphony of analog building blocks, each a vital component in the intricate tapestry of signal processing.

Function of Exponential Circuit

In this part, a new approximation function is presented to optimize the range of the Taylor series in order to implement the exponential circuit. This is because of fact that the conventional Taylor series is complicated to realize the circuit, and the other hand many terms are required to enhance the accuracy of the circuit. The proposed equation which resulted in MATLAB is:

$$\exp(x) = 1.45 x^2 + 0.12x + 1.24 \quad (9)$$

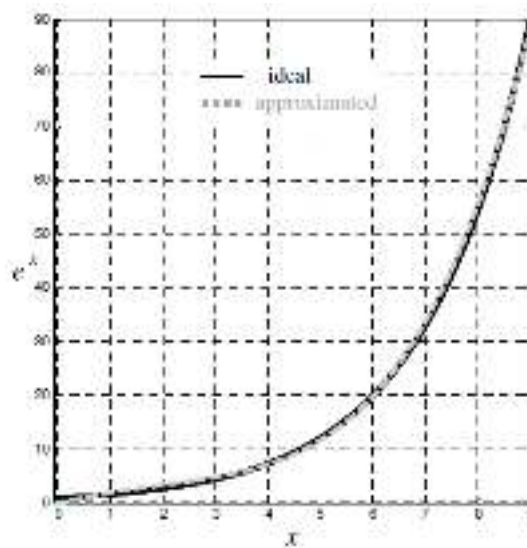


Fig. 3. Exp obtained via approximation method .

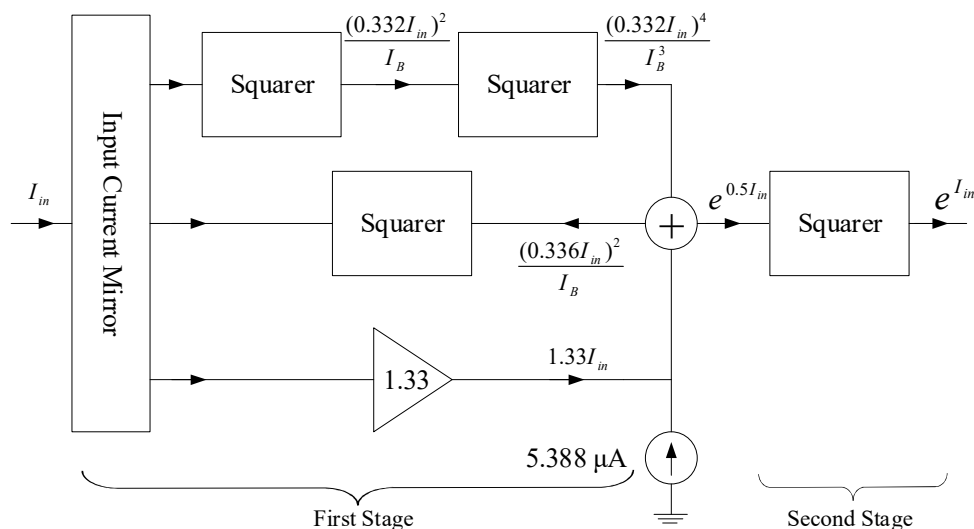


Fig. 4. The circuit for implementing the Exp.

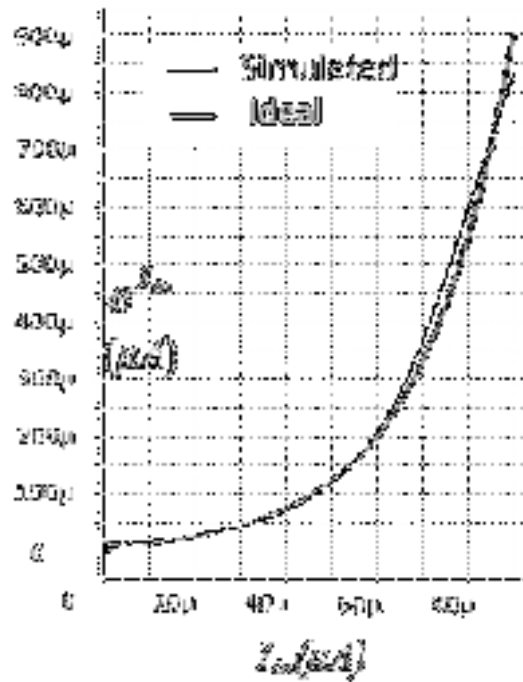


Fig. 5. The results of EXPFG a) input vs. output and b) The error results.

Logarithmic Function

For logarithmic function, again we used the same procedure which employed for exponential function, where the resulted function equation is:

$$\ln(x) = -0.07x^2 + 0.78x - 0.67 \quad (10)$$

The output of MATLAB depicted in the following figure, which circuit simulation results in the figure 8 verify achievement of design.

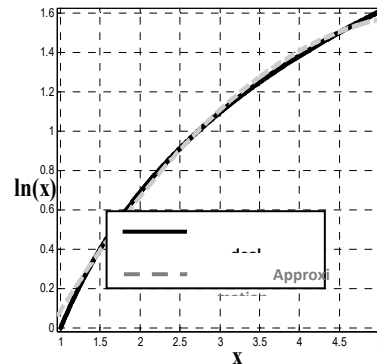


Fig. 6. LOG function via software.

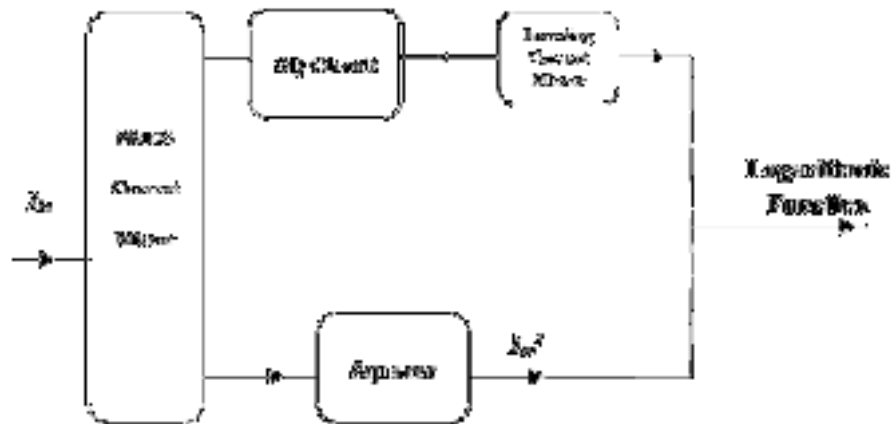


Fig. 7. The implemented of LOG function.

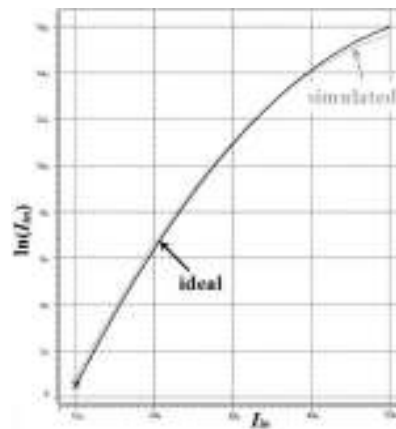


Fig. 8. Input vs. output of LOG function.

Analog Multiplier

The principle underpinning the operation of this multiplier is rooted in the synergy between the "basic cell" and the square-difference identity:

$$(X + Y)^2 - (X - Y)^2 = 4XY \quad (11)$$

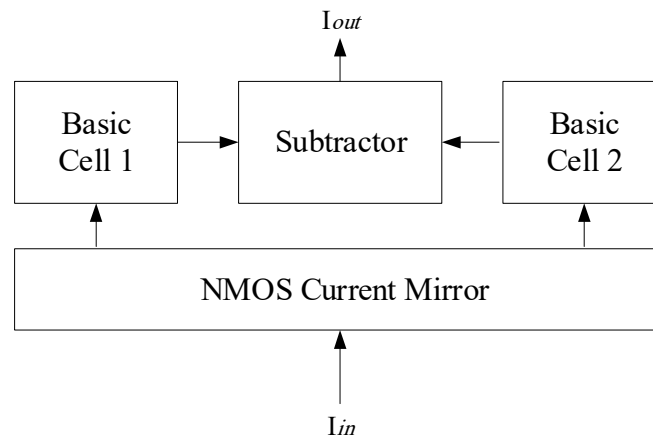


Fig. 9. The multiplier circuit by employing two "basic cell".

Behold the realization multiplication in analog mode, depicted at the illustrious Fig. 9. This architectural marvel is predicated upon the harmonious interplay of two loops of translinear.

$$I_{DS3} = \frac{I_{SQ}}{4} + I_x + I_b \quad (12)$$

$$I_{DS4} = \frac{I_{SQ}}{4} - I_x + I_b \quad (13)$$

$$I_{out} = \frac{I_{in}^2}{I_{norm}} \quad (14)$$

$$\ln(x) = -0.07x^2 + 0.78x - 0.67 \quad (15)$$

As the eloquence of (15) unveils, this intricate configuration results multiplier function of two current of I_x by I_y , their subsequent divided via bias current. DC transfer of function are showcased in the resplendent Fig. 10, a testament to its precision and performance.

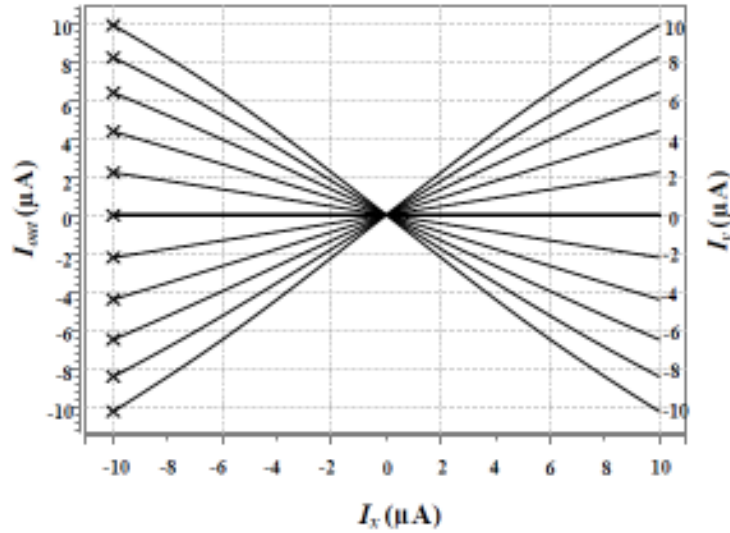


Fig. 10. Simulated result of multiplier.

Divider Function

Turning our attention to (15) once more, we uncover the inherent potential for division. By judiciously maintaining the current I_y (or I_x) as a continual, which is depicted in Fig. 9. Thus, the divider function is revealed, a paradigm that necessitates a prudent consideration. The multiplier circuit's ability to seamlessly transition into a divider function is elegantly portrayed in Fig. 11. With I_y normalized to unity, and for various quantities in I_x , emerges of I_{out} as well as the bis current, unveiling the circuit's versatility and adaptability.

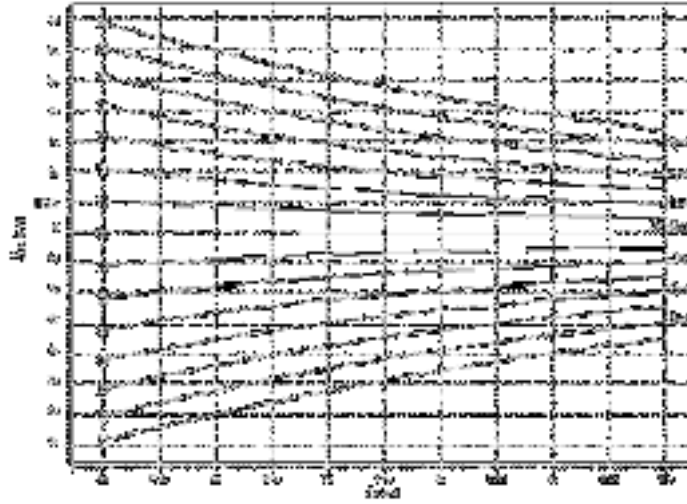


Fig. 11. Function of division in the simulation mode.

Examination of Main Circuit

The examination of main circuit, in terms of channel length modulation and Input range are presented in this section.

Mismatch of Threshold Voltage

The analysis considers the mismatch in voltage of threshold (Δ) at the transistors in the trans linear. The corresponded voltages are given as $V_{SGn} = V_{tn} + \Delta V_n$, Where $V_{tn} = V_t + \delta_n$. considering equation (4) we can derive:

$$I_{O1}'' \approx \frac{I_{x+y}^2 + 2\Delta k I_B I_{x+y}}{4I_B + 2\Delta k I_{x+y}} \quad (16)$$

$$V_{SG1} + V_{SG2} + \Delta_{12} = V_{SG3} + V_{SG4} + \Delta_{34} \quad (17)$$

Supposing $\Delta_{12} - \Delta_{34} = \Delta$, then:

$$\begin{aligned} 4I_B I_{out} \Delta - 4I_B^2 - 2I_B \Delta^2 - \\ 8I_B \Delta + 4I_B I_{out} \Delta^4 - 2I_B \Delta^3 + I_{out} \Delta^2 - 4I_B^2 \Delta^2 = I_{in}^2 \end{aligned} \quad (18)$$

Because Δ is very small (< 10 mV), then Δ^2 , Δ^3 and Δ^4 can be negligible. The output can be derived as:

$$I_{out} = \frac{I_{in}^2}{4I_B(1+\Delta)} + \frac{I_B + 2\Delta}{1+\Delta}$$

(19)

Considering $1 \gg \Delta$, the output of “*basic cell*” is:

$$I_{out} \approx \frac{I_{in}^2}{4I_B} + I_B + 2\Delta \quad (20)$$

Channel-Length Modulation

Channel-Length Modulation can be presented as the following equation:

$$I_{DS} = K(V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \quad (21)$$

In this equation, λ introduce the modulation coefficient. It is obvious that with low V_{DS} , this effect becomes low. In our proposed circuit, because of employing long length for transistors, hence this error can be considered negligible.

Examination of Signal Range at the Input

The signal quantities of the main circuit are limited via trans linear, including transistors transistor M1 as well as the M4, which operates in saturation regime which is expressed as[16]:

$$2\sqrt{I_B} \geq \sqrt{(1-\beta)I_B + \frac{\beta^2 I_B}{4}} + \sqrt{(1+\beta)I_B + \frac{\beta^2 I_B}{4}} \quad (22)$$

Considering $I_{in}=XI_B$ and then substituting equation (8) in equation (22), the parameter of X which is maximum value for the circuit is obtained:

$$2\sqrt{I_B} \geq \sqrt{\frac{X^2 I_B^2}{4I_B} + I_B + XI_B} + \sqrt{\frac{X^2 I_B^2}{4I_B} + I_B - XI_B} \quad (23)$$

By solving above equation, $X=$ and, $X=\pm 2$ where the value of $X=+2$ is right, hence:
 $I_{in} \leq 2I_B$

Thus, the range of input signal is restricted to $2I_B$.

In summary, the key points are:

1. Threshold voltage mismatch cause to output offset, which is paied back in adjusting the bias current.
2. Channel-length modulation is negligible due to the use of long-channel transistors.
3. The input current range is limited to twice the bias current to maintain transistor saturation in the dual translinear loop.

The analysis provides insights into the non-ideal effects and input limitations of the "basic cell" circuit, which is important for its practical implementation and performance.

Conclusion

In this scholarly endeavor, the exploration delved into the myriad applications of a CMOS squaring circuit within the realm of analog signal processing. This circuit, christened the "basic cell", was harnessed as the foundational element for the implementation in the logarithmic of input, division of two signal, multiplication, and exponential shape of circuit, each a testament to its versatility. Moreover, the paper unveiled a novel compound of the realization of analog logarithmic and exponential functions, characteristics that have proven elusive within the confines of CMOS technology. This ingenious solution encompassed the seamless integration of these functions into a configurable cell, a feat that exemplified the synergy between innovation and practicality. The circuits were brought to life through a current-mode realization, an approach that bestowed upon them a simplicity and intuitive nature, qualities that are coveted in the realm of design and implementation. The proposed circuits underwent a meticulous design and simulation process, facilitated by the HSPICE simulator, a powerful tool that leveraged the parameters of BSIM3v3 in the complementary of MOS transistor. This rigorous process ensured the circuits' adherence to industry standards and paved the way for their practical realization. To further validate the integrity of the simulation results obtained from HSPICE, the researchers employed MATLAB, a renowned computational software, to verify and corroborate the findings. This cross-validation ensured the robustness and reliability of the proposed circuits, reinforcing their potential for real-world applications.

REFERENCES

- Yang, Ziyun, Zichi Wang, and Xinpeng Zhang. "A general steganographic framework for neural network models." *Information Sciences* 643 (2023): 119250.
- Vohra, Sahibia Kaur, et al. "Circuit implementation of on-chip trainable spiking neural network using CMOS based memristive STDP synapses and LIF neurons." *Integration* 95 (2024): 102122.
- Jooq, Mohammad Khaleqi Qaleh, et al. "A high-performance and ultra-efficient fully programmable fuzzy membership function generator using FinFET technology for image enhancement." *AEU-International Journal of Electronics and Communications* 163 (2023): 154598.
- Naderi, Ali, et al. "A new high speed and low power four-quadrant CMOS analog multiplier in current mode." *AEU-International Journal of Electronics and Communications* 63.9 (2009): 769-775.
- Sajjadi-Kia, Hamed. "An analog cell and its applications in analog signal processing." *International Journal of circuit theory and applications* 39.2 (2011): 195-201.
- Saatlo, Ali Naderi, and Serdar Ozoguz. "CMOS design of a multi-input analog multiplier." *PRIME 2012; 8th Conference on Ph. D. Research in Microelectronics & Electronics*. VDE, 2012.
- Nivedha, S., and M. Bhaskar. "Dual-tuned high-swing variable-gain amplifier with enhanced dB-linear control." *AEU-International Journal of Electronics and Communications* 175 (2024): 155079.
- Tanno, Koichi, Okihiko Ishizuka, and Zheng Tang. "Four-quadrant CMOS current-mode multiplier independent of device parameters." *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 47.5 (2000): 473-477.

- Aghaei, Tohid, and Ali Naderi Saatlo. "A new strategy to design low power translinear based CMOS analog multiplier." *Integration* 69 (2019): 180-188.
- Naderi, A., et al. "Circuit implementation of programmable high-resolution rational-powered membership functions in standard CMOS technology." *IEEE EUROCON 2009*. IEEE, 2009.
- S Minaei, Shahram, and Erkan Yüce. "New squarer circuits and a current-mode full-wave rectifier topology suitable for integration." (2010).
- Saatlo, Ali Naderi. "Systematic design of stable high-order delta sigma modulators using genetic algorithm." *Analog Integrated Circuits and Signal Processing* 118.1 (2024): 15-24.
- Gardeshkhah, Rasool, and Ali Naderi Saatlo. "A New Tunable Gyrator-C-Based Active Inductor Circuit for Low Power Applications." *Journal of Circuits, Systems and Computers* 32.13 (2023): 2350235.
- Saatlo, A. N., Ozoguz, S., & Minaei, S. "Applications of a CMOS current squaring circuit in analog signal processing". In *2015 38th International Conference on Telecommunications and Signal Processing* 14.3(2015): 339-343.
- Aghaei, Tohid, Hassan Faraji Baghtash, and Ali Naderi Saatlo. "A translinear principle based low-power high-precision RMS-to-DC converter in CMOS technology." *Analog Integrated Circuits and Signal Processing* 111.1 (2022): 45-56.
- Aghaei, T., and A. Naderi. "A New Highly Accurate Translinear Based CMOS Multiplier in Current Mode with Low Power Dissipation." *TABRIZ JOURNAL OF ELECTRICAL ENGINEERING* 50.2 (2020): 517-529.